AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-22 (Cancelled)

23. (Original) A semiconductor integrated circuit device comprising:

(a) three or more element forming regions formed on a surface of a semiconductor substrate and defined by an insulating film, said three or more element forming regions each extending in a first direction and being arranged in a second direction perpendicular to said first direction;

(b) a plurality of memory cells formed on each of said element forming regions, said memory cells each including:

(b_1) a first electrode constituted by a first conductive film formed through a first insulating film;

(b_2) a second electrode constituted by a second conductive film formed through a second insulating film on said first electrode, said second electrode extending in said second direction; and

(b_3) semiconductor regions formed on the element forming region on both sides of said second electrode,

wherein pseudo memory cells formed on an outermost element forming region out of said three or more element forming regions do not function as memory cells, and

wherein a semiconductor region of said pseudo memory cells is connected with ground potential.

24. (Original) A semiconductor integrated circuit device according to claim 23, wherein said second conductive film is in a floating state.

25. (Original) A semiconductor integrated circuit device according to claim 23, wherein said semiconductor region of said pseudo memory cells is in an OFF state.

26. (Original) A semiconductor integrated circuit device according to claim 23, wherein a connecting portion extending in said second direction is provided to connect end portions of said three or more element forming regions.

27. (Original) A semiconductor integrated circuit device according to claim 26, wherein said second conductive film is in a floating state.

28. (Original) A semiconductor integrated circuit device according to claim 26, wherein said semiconductor region of said pseudo memory cells is in an OFF state.

29. (Original) A semiconductor integrated circuit device according to claim 23, wherein said three or more element forming regions are arranged in said second direction perpendicular to said first direction, and

wherein a width in said second direction of an outermost element forming region out of said three or more element forming regions is larger than a width in said second direction of each of the other element forming regions.

30. (Original) A semiconductor integrated circuit device according to claim 29, wherein said second conductive film is in a floating state.

31. (Original) A semiconductor integrated circuit device according to claim 29, wherein said semiconductor region of said pseudo memory cells is in an OFF state.